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TREAT, WILLIAM M

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

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Applicants' most recent response continues to be non-responsive in the examiner's judgement. The examiner makes this statement for the following reasons.

I. The restriction requirement as explained by the examiner is valid. Therefore, by cancelling all claims to the original invention, only submitting claims to a new invention, and refusing to cancel the claims to the new invention and submit claims to the original invention, applicants are being non-responsive.

II. Applicants have incorrectly argued (a) the original invention and the new invention are not seperate and distinct and (b) "machine specific register" has been defined as a synonym for registers associated with processor functional units in the original application meaning that when the phrase, "registers associated with processor functional units", was used in the original claims, applicants were claiming machine specific registers.

As to the validity of the restriction requirement, applicants have what are, essentially, three independent inventions described in their specification. A first invention, originally claimed by applicants, accomplishes a given task by direct triggering of the processor logic without use of machine specific registers. On page 5, line 25 through page 6, line 4, applicants state: "Fig. 2B is a block diagram of an alternate embodiment of the processor shown in Fig. 1 and external microcode stored in a computer readable medium. In one embodiment of the invention, a computer readable medium 220, which is external to the processor, stores program 222 for controlling the operation of the processor 224. Examples of computer readable mediums external to the processor include, but are not limited to, mass storage devices, firmware, and memory. The programmed code 222 stored in the computer readable medium is referred to herein as 'external microcode.' In an example embodiment, the external microcode 222 implements microcode operations by controlling hardware logic on the processor 224 without the use of the registers (i.e., the machine specific registers) shown in Fig. 2A." Applicants' original claims were all directed to the invention which "implements microcode operations by controlling hardware logic on the processor 224 without the use of the registers (i.e., the machine specific registers) shown in Fig. 2A." A second invention accomplishes the given task using just machine specific registers. On page 4, line 25 through page 5, line 3, applicants state: "Fig. 2A is a more detailed block diagram of an example embodiment of the processor and firmware shown in Fig. 1. In one embodiment of the invention, firmware 206 stores program code 210 for controlling the operation of the processor 204. The programmed code 210 stored in the firmware 206 is referred to herein as the 'firmware code.' In an example embodiment, the firmware code 210 implements microcode operations using registers which are specific to a particular machine or to a particular model of a machine. The registers are referred to herein as 'Machine Specific Registers.' The machine specific registers function as an interface between the firmware 206 and the processor 204." Applicants' claims 21-40 are all directed to the invention of the embodiment requiring machine specific registers. A third invention accomplishes the given task using a combination of machine specific registers and direct triggering of the hardware processor logic. On page 6, lines 6-8, applicants state: "In still another embodiment, the external microcode

222 implements microcode operations by a co[redacted]nation of using the registers shown in Fig. 2A[redacted], the machine specific registers) and by directly triggering the processor hardw[redacted]logic." Amended claim 10, which effectively [redacted]cels original claim 10, is directed to the invention of this third embodiment. One invention has A,B,(not C). A second invention has A,C, (not B), and a third invention has A,(B in combination with C). If a condition of your invention is (not C) as in A,B,(not C), then such an invention is clearly independent of one requiring C as in A,C, (not B) or A,(B in combination with C). If a condition of your invention is (not B) as in A,C, (not B), then such an invention is clearly independent of inventions requiring B as in A,B, (not C) and A,(B in combination with C). If a condition of your invention is (B in combination with C) as in A, (B in combination with C), then such an invention is clearly independent of an invention requiring (not B) as in A,C, (not B) and an invention requiring (not C) as in A,B, (not C). Furthermore, there is a clear burden on the examiner. Art which required the given task be accomplished using machine specific registers or using a combination of both machine specific registers and the techniques used for directly triggering the processor hardware logic would not meet the limitation of the first invention which accomplishes the task without any use of machine specific registers. The art, without machine specific registers, used to successfully reject applicants' original claims does not read on the embodiments which require any use of machine specific registers. The inventions are independent and represent a burden on the examiner to search. Furthermore, since applicants purposely omitted any mention of machine specific registers from their original claim languge, the examiner was compelled to find art appropriate to the first invention which omits machine specific registers, entirely.

As to applicants' argument the term, "machine specific register", is synonomous with the phrase, "registers associated with processor functional units", this was considered by the examiner but has no merit. Were we to accept applicants' argument that registers associated with a functional unit are "machine specific registers" then prior art general purpose registers used by a functional unit would be "machine specific registers" since they must be associated with a functional unit through logic and electrical connection to perform any work in conjunction with a functional unit. Prior art pipeline registers which hold intermediate values at intermediate stages of a functional unit's pipeline would be "machine specific registers" because they are an integral part of a functional unit's circuitry and, therefore, must be associated with a processor functional unit. However, when one reads applicants' specification (page 7, lines 21-23), it is clear applicants do not intend that general purpose registers will be machine specific registers. And, when one of ordinary skill reads the other examples of machine specific registers and their related description in applicants' specification, it is clear that pipeline registers holding intermediate values at intermediate stages in functional unit pipelines are not machine specific registers though they are hard-wired, integral components of prior art processors with functional units. As pointed out by the examiner in paper no. 13, mailed on 2/6/03, the applicants have taken a nebulous phrase and tried to argue it has specific meaning which makes no sense within the art. Nor, can applicants find an English language or computer dictionary which would support their argument for such a narrow definition of the phrase, registers associated with processor functional units. In fact, without significant additional description from applicants' specification, one of ordinary skill would not know what applicants actually meant by machine specific registers nor could applicants distinguish over prior art.

In view of applicants' unwillingness to present claims to the invention originally elected and their petition traversing the restriction, the examiner has forwarded the application to the appropriate deciding authority.

WILLIAM M. TREAT
PRIMARY EXAMINER